REMARKS

Reconsideration and allowance of this application are respectfully requested. Claims 11-20 remain pending, where claims 1-10 were previously cancelled and claims 11-12 are withdrawn. By this communication, no new claims are added or cancelled, and claims 13, 15, 17, and 18 are amended.

Election/Restriction

On July 24, 2008, via a telephone conversation, the Examiner informed Applicants' representative that he was imposing a restriction requirement, and to request that Applicants elect one of two identified inventions (Invention I, comprising claims 11-12 and Invention II, comprising claims 13-20) for prosecution in connection with the present application. On July 25, 2008, Applicants' representative orally elected Invention II, comprising claims 13-20.

In the Office Action dated August 1, 2008, rather than restating the restriction requirement that was orally presented to Applicants' representative, an election of species requirement is set forth. Applicants traverse the election requirement as set forth in the Office Action, since it improperly characterizes the subject matter of Figures 1 and 15 as being "mutually exclusive" species. The Office Action does not set forth any basis for this characterization.

Figure 1 is a block diagram of portions of a design support apparatus. One of the elements of this apparatus is a data analyzing unit 9. Figure 15 is a diagram that explains the input and output information of the data analyzing unit 9. In other words, Figure 15 provides a more detailed explanation of one of the components of the apparatus of Figure 1. The Office Action has not established any feature of Figure 15 that would not also be found in the apparatus of Figure 1. Accordingly, there is no showing of "mutually exclusive

characteristics" that is necessary to support an election of species requirement. For this reason, the election of species is traversed.

The Examiner is requested to clarify for the record whether a restriction requirement is being imposed, as stated to Applicants' representative during the telephone call, or an election of species requirement, as set forth in the Office Action. If it is to be a restriction requirement, then Applicants are entitled to an explanation of the reasons that the two groups of claims are considered to be materially distinct, so that they can determine whether the restriction should be traversed. If, on the other hand, the Examiner intended an election of species, then an explanation of the mutually exclusive characteristics of Figures 1 and 15 must be provided. In the absence of the appropriate showing, the requirement should be withdrawn.

Specification Objection

The title of the claimed invention is objected to for allegedly being non-descriptive. Applicants have amended the title to be a more descriptive title. Accordingly, Applicants respectfully request that the objection to the specification be withdrawn.

Drawings Objection

The drawings are objected to because the input and output of blocks [2] and [9], respectively, are not labeled. Applicants have amended Figure 1 to include the input and output of blocks [2] and [9], respectively. Applicants respectfully request that the objection to the drawings be withdrawn.

Rejection Under 35 U.S.C. §112

Claim 13 stands rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to point out and distinctly claim the subject matter of the invention. In particular,

the Office asserts that the limitations "fluctuation arrangement" and "arranging the semiconductor chip on an interposer" are unclear. Applicants have amended claim 13 to more clearly recite the aforementioned features. Accordingly, Applicants respectfully request that the rejection to claim 13 under 35 U.S.C. §112, second paragraph be withdrawn.

Rejections Under 35 U.S.C. §102

Claims 13-20 - *Ding*

Claims 13-20 stand rejected under 35 U.S.C. §102(b) for alleged anticipation by *Ding et al.* (U.S. Patent No. 5,801,959, hereinafter *Ding*). Applicants respectfully traverse this rejection.

Ding discloses producing a dense layout that enables an integrated circuit design to be implemented on a smaller semiconductor die resulting in a size reduction in the final packaged integrated circuit. *Ding*, col. 2, lines 35-40. *Ding* further discloses combining routing space estimation and adjustment (a technique similar to channel-based global routing) with area-based detailed routing to produce the layout. *Id.*, col. 2, lines 40-43.

An integrated circuit design is developed that includes specification of particular components (cells and blocks) as well as the interconnections that must be made between various components. *Id.*, col. 2, lines 47-50. Most of the components include at least one pin for accepting an input electrical signal to the component and many also include at least one additional pin for providing an output electrical signal from the component. *Id.*, col. 2, lines 50-54. The interconnections are made between pins of different components. *Id.*, col. 2, lines 54-55.

Once the integrated circuit design has been established, the layout of the components and interconnections of the design are determined so that the components and interconnections can be produced on the surface of a semiconductor die. *Id.*, col. 2, lines 56-

60. Sometimes, the integrated circuit design must be implemented on a die of a specified size (i.e., having a particular surface area). *Id.*, col. 2, lines 60-62. Other times, the approximate size of the die required to implement the integrated circuit design can be estimated. *Id.*, col. 2, lines 62-64. In any event, a die size is assumed prior to beginning determination of the integrated circuit layout. *Id.*, col. 2, lines 64-65.

Ding further discloses a method for determining an integrated circuit layout on a surface of a semiconductor die that includes the steps of: i) determining the placement of each component on the die surface, ii) performing routing space estimation and adjustment to approximately define the routing demand, and iii) performing area-based detailed routing to exactly define the path of each interconnection on the die surface. *Id.*, col. 2, line 66 through col. 7, line 6. Together, the routing space estimation and adjustment step and the component placement step define a die size that may or may not be the same as the die size specified prior to implementing the layout method. *Id.*, col. 2, lines 6-10.

As discussed above, *Ding* discloses routing and adjustment techniques for a more dense layout of integrated circuit components on a semiconductor die. However, nowhere in *Ding* is there disclosed using bond wires or simulation data obtained from bond wiring. Accordingly, *Ding* does not disclose at least "a second data creating unit that creates, based on the design data of the semiconductor package and the semiconductor chip simulated arrangement data, bond wire simulation data obtained by wiring, using bond wires, the bond wire connection terminals of the semiconductor chip arranged to deviate from an arrangement position in the design data and bond wire connection terminals of the interposer" as recited in independent claim 13.

Because *Ding* fails to disclose each and every feature of the claimed invention, *Ding* cannot anticipate or render the claimed invention as recited in claim 13 obvious to one skilled

in the art. Claims 14-20 are also allowable by virtue of their dependency from independent claim 13, and for the features recited therein.

Accordingly, Applicants respectfully request that the rejection to claims 13-20 under 35 U.S.C. § 102(b) be withdrawn.

Claim 13 - *Razon*

Claim 13 stands rejected under 35 U.S.C. §102(b) for alleged anticipation by *Razon et al.* (U.S. Patent No. 5,950,070, hereinafter *Razon*). Applicants respectfully traverse this rejection.

Razon discloses a method of assembling a plurality of semiconductor chips. *Razon*, Abstract. Each of the plurality of chips has a contact pattern area including a pattern of contacts on a surface of the chip. *Id.* A respective section of a dielectric interposer is assembled to each respective one of the plurality of chips individually, without detaching the plurality of chips from the portion of the semiconductor wafer. *Id.* Each section of interposer has a plurality of bonding pads near an outer periphery of the section, so that each bonding pad lies near the contact pattern area of the corresponding one of the plurality of chips. *Id.* Each bonding pad is wire bonded to a respective one of the contacts on the front surface of the corresponding one of the plurality of chips. *Id.*

A plurality of individual interposer (tape) sections are provided for attachment to the dies. *Id.*, col. 4, lines 45-46. In general, each section of the respective interposer has a plurality of bonding pads located around the perimeter of the interposer, a plurality of lands for receiving solder balls, and a respective lead connecting each bonding pad of the interposer to a respective solder ball land. *Id.*, col. 4, lines 52-64.

As discussed above, *Razon* discloses a method of assembling a semiconductor chip package, but does not disclose creating simulated arrangement data obtained from the

positioning of the semiconductor chip. The Office, in asserting that *Razon* teaches this aforementioned feature, states that "an alignment chip on the interposer controls whether each one of the electrical connections (e.g., bondwires) between terminals of the interposer and the contacts of the chip can be made successfully without great difficulty." (*See* Office Action at 24, pg. 10). However, *Razon* does not disclose an "alignment chip" being on the interposer, but rather a plurality of bonding pads, a plurality of lands for receiving solder balls, and respective leads connecting each bonding pad to a respective solder ball (*See Razon*, col. 4, lines 51-64). Accordingly, *Razon* does not disclose at least "a first data creating unit that creates, based on design data of a semiconductor package, semiconductor chip simulated arrangement data obtained by arranging a semiconductor chip onto the surface of an interposer such that deviation of the semiconductor chip from an original position is simulated" as recited in independent claim 13.

Because *Razon* fails to disclose each and every feature of the claimed invention, *Razon* cannot anticipate or render the claimed invention as recited in claim 13 obvious to one skilled in the art.

Accordingly, Applicants respectfully request that the rejection to claim 13 under 35 U.S.C. § 102(b) be withdrawn.

Claims 13-20 - *Howard*

Claims 13-20 stand rejected under 35 U.S.C. §102(e) for alleged anticipation by *Howard et al.* (U.S. Patent No. 7,132,359, hereinafter *Howard*). Applicants respectfully traverse this rejection.

Howard discloses wirebonding methods in which bondwires are positioned using dynamically determined variations in die placement. *Howard*, Abstract. A die is placed on a prepared substrate using selected ideal placement coordinates. *Id.* Deviation of the actual die

placement from the selected idea placement coordinates is monitored, and one or more critical bondwires are wirebonded between respective die pins and pins on the substrate. *Id.* The monitored placement deviation is used to dynamically position the critical bondwires on the critical pins according to actual die placement. *Id.*

As discussed above, *Howard* discloses a method and device for improving precision in wirebonding by dynamically accounting for variation in die placement and implementing bondwire attachment accordingly. However, *Howard* does not disclose the aforementioned in the use of an interposer. Accordingly, *Howard* does not disclose at least "a first data creating unit that creates, based on design data of a semiconductor package, semiconductor chip simulated arrangement data obtained by arranging a semiconductor chip onto the surface of an interposer such that deviation of the semiconductor chip from an original position is simulated" as recited in independent claim 13.

Because *Howard* fails to disclose each and every feature of the claimed invention, *Howard* cannot anticipate or render the claimed invention as recited in claim 13 obvious to one skilled in the art. Claims 14-20 are also allowable by virtue of their dependency from independent claim 13, and for the features recited therein.

Accordingly, Applicants respectfully request that the rejection to claims 13-20 under 35 U.S.C. § 102(e) be withdrawn.

Conclusion

Based on at least the foregoing amendments and remarks, Applicants submit that claims 13-20 are allowable, and that this application is in condition for allowance. Accordingly, Applicants request a favorable examination and consideration of the instant application. In the event the instant application can be placed in even better form, Applicants request that the undersigned attorney be contacted at the number below.

Respectfully submitted,

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ANNOTATED SHEET
Appln. Filing Date: July 24, 2006
Title: DESIGN SUPPORT APPARATUS FOR SEMICONDUCTOR DEVICES
Inventor(s): Akihiro Goto et al.
Atty. Dkt. No.: 1032404-000154 Sheet 1 of 1

FIG.1